Customer No.: 31561
Application No.: 10/707,015
Docket NO.: 10542-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A process for fabricating a substrate, at least comprising the steps of

providing a semi-finished substrate having a plurality of insulating layers and a plurality of patterned metallic layers alternately stacked over each other, wherein the patterned metallic layers are electrically interconnected, the two outermost insulating layers in the semi-finished substrate are defined as a first insulating layer and a second insulating layer, two inner patterned metallic layers are defined as a first patterned metallic layer and a second patterned metallic layer, the first insulating layer and the second insulating layer cover the first patterned metallic layer and the second patterned metallic layer respectively, and the first insulating layer and the second insulating layer have a plurality of first openings and a plurality of second openings that expose the first patterned metallic layer and the second patterned metallic layer respectively;

forming a first seed layer on the first insulating layer and in the first openings and forming a second seed layer on the second insulating layer and in the second openings;

forming a first mask layer and a second mask layer over the first seed layer and the second seed layer and patterning the first mask layer and the second mask layer to form a plurality of first patterned openings and a plurality of second patterned openings, wherein the first patterned openings and the second patterned openings expose the first openings and the second openings respectively;

depositing a first metal and a second metal into the first openings and the second openings to form a first metallic layer and a second metallic layer respectively, wherein the first metallic layer and the second metallic layer are positioned over the first seed layer and the second seed layer, and the second metallic layer is partially filled into the second patterned opening in the second mask layer;

removing the first mask layer and the second mask layer;

forming a third mask layer over the first seed layer and the first metallic layer and forming a fourth mask layer over the second seed layer and the second metallic layer, wherein the third mask layer has a plurality of third patterned openings that exposes the first seed layer and the first metallic layer;

forming a plurality of circuit lines inside the third patterned openings such that the circuit lines are positioned over the first seed layer and the first metallic layer;

removing the third mask layer and the fourth mask layer;

removing the exposed first seed layer and the second seed layer;

forming a first solder mask layer and a second solder mask layer on the first insulating layer and the second insulating layer, wherein the first solder mask layer and the second solder mask layer has a plurality of first solder mask openings and a plurality of second solder mask openings, and the first solder mask openings at least expose a portion of the circuit lines and the second solder mask openings expose the second metallic layer;

forming a third seed layer on the first solder mask layer, in the first solder mask openings and on the circuit lines exposed by the first solder mask openings and forming a fourth seed layer on the second solder mask layer and on the second metallic layer;

forming a fifth mask layer over the third seed layer such that the fifth mask layer has a plurality of fourth patterned openings that exposes the first solder mask openings and forming a sixth mask layer over the fourth seed layer;

forming a plurality of contacts inside the first solder mask openings above the third seed layer such that the contacts and the circuit lines are electrically connected;

removing the third mask layer and the fourth mask layer; and

removing the exposed third seed layer and the fourth seed layer.

2. (original) The substrate fabrication process of claim 1, wherein the step of forming the first seed layer and the second seed layer on the first insulating layer and the second insulating layer is performed by an electroless plating operation.

3. (original) The substrate fabrication process of claim 1, wherein the step of forming the circuit lines inside the third patterned openings is performed by an electroplating operation.

4. (original) The substrate fabrication process of claim 1, wherein the step of forming the first solder mask layer and the second solder mask layer on the first insulating layer and the second insulating layer is performed by a screen printing operation.

5. (original) The substrate fabrication process of claim 1, wherein the step of forming the third seed layer and the fourth seed layer is performed by an electroless plating operation.

6. (original) The substrate fabrication process of claim 1, wherein the step of forming the contacts inside the first solder mask openings is performed by an electroplating operation.

7. (original) A process for fabricating a substrate, at least comprising the steps of:

providing a semi-finished substrate including a plurality of insulating layers and a plurality of patterned metallic layers alternately stacked over each other such that the patterned metallic layers are electrically interconnected, wherein at least one of the insulation layers is located on a surface of the semi-finished substrate and defined as a surface insulating layer;

forming at least a circuit line on the surface insulating layer such that the circuit line and the patterned metallic layers within the substrate are electrically connected;

forming at least a solder mask layer over the surface insulating layer, wherein the solder mask layer has at least an opening that exposes the circuit lines; and

forming a contact within the opening of the solder mask layer such that the contact and the circuit line are electrically connected.

8. (original) The substrate fabrication process of claim 7, wherein the step of forming the circuit line on the semi-finished substrate comprises:

performing an electroless plating operation to form a seed layer over the surface insulating layer, wherein the seed layer and the patterned metallic layers within the semi-finished substrate are electrically connected;

forming a mask layer over the seed layer and patterning the mask layer to form a patterned opening;

performing an electroplating operation to form the circuit line within the patterned opening;

removing the mask layer; and

removing the exposed seed layer.

9. (original) The substrate fabrication process of claim 7, wherein the step of

forming the solder mask layer over the surface insulating layer is performed by a screen printing operation.

10. (original) The substrate fabrication process of claim 7, wherein the step of forming the contact inside the opening of the solder mask layer comprises:

performing an electroless plating operation to form a seed layer on the solder mask layer, in the opening in the solder mask layer and on the circuit line such that the seed layer and the circuit lines are electrically connected;

forming a mask layer on the seed layer and patterning the mask layer to form at least a patterned opening that exposes the opening in the solder mask layer;

performing an electroplating operation to form the contact within the opening of the solder mask layer such that the contact and the seed layer are electrically connected;

removing the mask layer; and

removing the exposed seed layer.

Claims 11-14 (canceled).